Description:

The Core Registers unit receives data from the wishbone slaves, samples it, and transmits it to the core blocks. When reset is activated no register should be enabled. The register's addresses are defined by generics.

The unit contains four registers which are configed as follow:

trigger\_type\_reg\_1 = trigger\_type

trigger\_position\_reg\_2 = trigger\_position

clk\_to\_start\_reg\_3 = clk\_to\_start

enable\_reg\_4 = enable

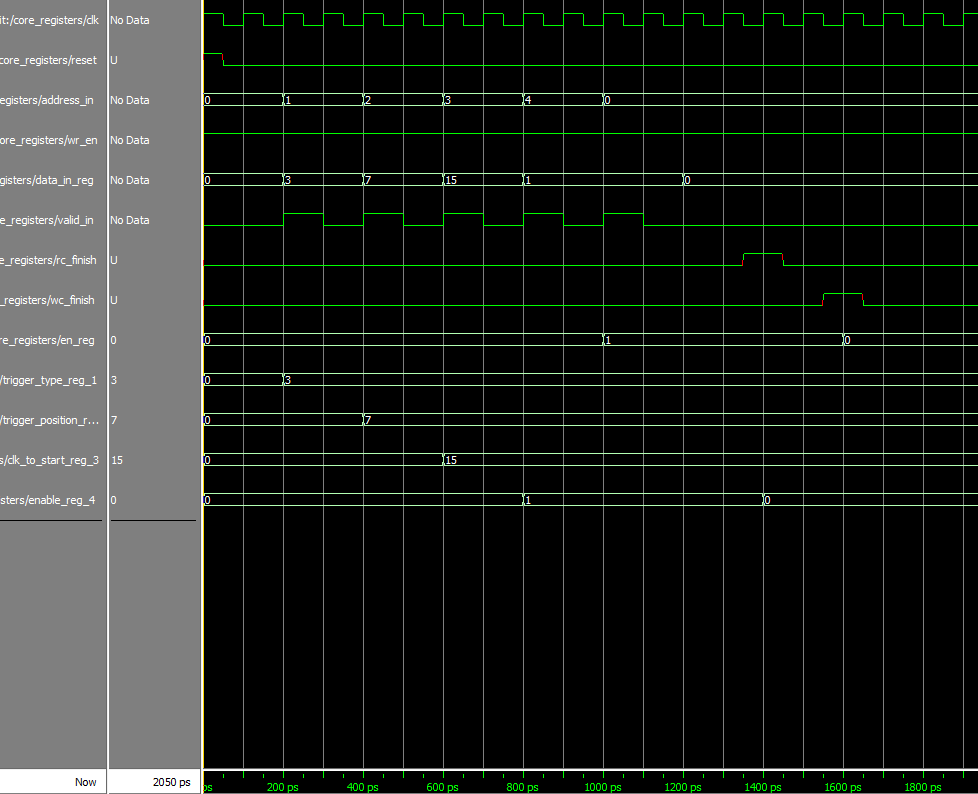
Generic table

|  |  |  |
| --- | --- | --- |
| Name | Width | Description |
| reset\_polarity\_g | 1 | '1' reset active high, '0' active low |
| enable\_polarity\_g | 1 | '1' the entity is active high, '0' entity is active low |
| data\_width\_g | 8 | defines the width of the data lines of the system |
| Add\_width\_g | 8 | width of addr word in the RAM |
| en\_reg\_address\_g | 1 | Enable the registers for reading |
| trigger\_type\_reg\_1\_address\_g | 1 | Address of the type register |
| trigger\_position\_reg\_2\_address\_g | 1 | Address of position register |
| clk\_to\_start\_reg\_3\_address\_g | 1 | Address of counter register |
| enable\_reg\_address\_4\_g | 1 | Address of enable register |

Signals table

|  |  |  |  |
| --- | --- | --- | --- |
| Name | Direction | Width | Description |
| clk | In | 1 | System clock |
| Reset | In | 1 | System reset |
| address\_in | In | Add\_width\_g | Address of the register that the data is writing to. (determine by the generics) |
| wr\_en | In | 1 | write enable: '1' for write, '0' for read |
| data\_in\_reg | In | data\_width\_g | data sent from WS to store in the registers |
| valid\_in | In | 1 | Data in valid |
| rc\_finish | In | 1 | When signal rise we reset enable register |
| wc\_finish | In | 1 | After write controller finish, we need to input a new configurations |
| en\_out | Out | 1 | Enable reading from registers |
| trigger\_type\_out\_1 | Out | 7 | Trigger type |
| trigger\_positionout\_2 | Out | 7 | Trigger position |
| clk\_to\_start\_out\_3 | Out | 7 | Trigger counter |
| enable\_out\_4 | Out | 1 | System enable |

Simulation



We can see a data that is written to each one of the registers. In addition we can see that after wc\_finish signal rise, the registers are not enabled- register number 0 is resetting into 0 (the configuration need to be enabled again), and when rc\_finish signal rise (system output all the data back to the user), the enable register is resetting back into 0, (register number 4).